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Visualizing electrothermal dynamics in ovonic threshold switches via in-situ thermoreflectance for enhanced reliability

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ABSTRACT

This study investigates the thermal behavior of Te-rich GeTe (GT)- and Se-doped GeTe (SGT)-based ovonic threshold switch (OTS) devices, focusing on understanding electrothermal dynamics and enhancing device reliability. Thermoreflectance-based thermal imaging (TTI) enables direct visualization of localized conductive channels, offering insights into heat localization during switching. Time-domain thermoreflectance (TDTR) further provides accurate thermal properties of the amorphous films, enabling electrothermal (ET) simulations. These simulations reveal that internal temperatures in GT-based devices may approach crystallization thresholds during operation, emphasizing the need for optimized thermal design. In contrast, SGT-based devices exhibit improved thermal stability, attributed to stronger bonding and reduced Joule heating, thereby maintaining their structural integrity during switching. The combination of experimental thermal mapping and predictive modeling offers a powerful framework for identifying potential failure points and guiding material design. By comparing GT and SGT systems, the study highlights how targeted doping strategies and current optimization can significantly improve thermal resilience and device durability. These findings provide a comprehensive understanding of thermal dynamics in OTS devices and demonstrate a path forward for the development of more robust and reliable selectors.

1. Introduction

To emulate human-like inferences, learning, and recognition in computing systems, large-scale integrated data storage devices are essential. Crossbar array (CA)-based data storage devices, known for their parallel memory structure, present a promising solution for high-density memory architectures due to their ability to execute extensive data processing with low power consumption, simple design, and high-integration density [1–3]. However, as memory density increases in CA structures, the issue of "sneak current" may arise, where current leakage through adjacent cells disrupts read and write operations, leading to reduced component durability and increased power consumption [4]. To address this sneak current problem, integrating nonlinear two-terminal selector devices stacked on individual memory elements has been proposed [5,6], prompting research into various types of selectors, such as PNP (NPN) junctions [7,8], Schottky-type diodes [9–11], tunneling selectors [12,13], mixed ion-electron conductors [14,15], metal-insulator transitions [16], and ovonic threshold switches (OTS). Among these, OTS devices have received significant attention due to their high nonlinearity, rapid operation speed, and proven reliability in conjunction with phase-change memory (PCM) [17].

OTS devices are two-terminal devices comprising an amorphous chalcogenide film sandwiched between top and bottom metal electrodes. The threshold switching (TS) phenomenon was first demonstrated by Ovshinsky in 1968 [18]. Initially, in a high-resistance state upon application of an external voltage, the device transitions rapidly to

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a low-resistance state upon exceeding a threshold voltage (V_{th}). When the external voltage is reduced below a certain threshold (V_{hold}), the device returns to the initial high-resistance state, exhibiting volatile resistance changes in response to voltage application. Recent studies have reported variations in V_{th} due to changes in the trap density within the bandgap of chalcogenide films under different pulse conditions [19,20]. Furthermore, these variations in V_{th} exhibit memory effects that depend on the applied voltage pulse conditions [21]. Due to this memory effect, OTS devices have garnered significant attention as selector-only memory (SOM) devices [21–24].

Extensive research on chalcogenide film materials for OTS device fabrication has been conducted [25], encompassing compositions ranging from single-component films, such as GeS [26,27], GeSe [28], SiTe [29], and Te-rich GeTe [30,31] to multicomponent films, such as Ge-S-As [32], Ge-Se-As [33], Ge-Se-Si [34], Ge-Te-As [35], and Ge-Te-As-Si [36]. Among these materials, we focus on Te-rich GeTe (GT)-based OTS devices due to their fast operation, excellent TS characteristics, good durability, and simple material structures. However, amorphous chalcogenide films based on GT present a challenge regarding thermal stability, as film crystallization occurs within the back-end-of-line process temperature range, potentially impacting both the manufacturing process and device operation [37]. Fundamentally, the TS phenomenon in chalcogenide film acts as a precursor to the PCM operation, generating a volatile conductive channel (CC) that eventually induces a phase change owing to Joule heating [38]. Consequently, heating from TS operation can degrade the device, negatively affecting its durability. In contrast to GT devices, Se-doped GeTe (SGT)-based OTS devices exhibit superior thermal stability, offering a solution to the issues. Therefore, we aimed to observe the heating process caused by TS behavior in real time and verify the internal temperature of GT devices during the TS process by monitoring current and surface temperature changes. Using the same approach, we analyzed SGT devices and conducted a comparative study with GT devices to identify the TS properties from a thermal perspective. In this study, we designated the compositions of GT and SGT thin films as $GeTe_5$ and $Se_3Ge_2Te_5$, respectively, and confirmed these compositions using X-ray fluorescence analysis as illustrated in Fig. S1.

Studies have reported heating during voltage application in two-terminal memory devices such as resistive random access memory (RRAM) and PCM using scanning thermal microscopy (SThM) [39–41]. However, SThM analysis requires horizontal device fabrication and deposition of an Al_2O_3 capping layer for contact protection during probe-tip contact. Furthermore, continuous voltage application during scanning demands stability to prevent device failure or deformation. This stability requirement can be challenging in the analysis of OTS devices with poor stability. Thermoreflectance-based thermal imaging (TTI) is another method involving irradiation of a device with light-emitting diode (LED) light during voltage pulse application. It detects changes in optical reflectivity due to heating, providing thermal images during operation [42,43]. TTI has been used to analyze thermal behavior during the Mott insulator–metal transition, offering direct observation of surface temperature in typical device structures [44,45]. Additionally, leveraging these measurements and values obtained from electrical and thermal property values experiments, electrothermal (ET) simulations based on the finite element method were conducted. These simulations predict the internal temperature of devices during TS operation and their failure mechanism. Therefore, this study provides insights into (1) the thermal dynamics and failure mechanisms of GT-based OTS devices and (2) a comparison of SGT-based OTS devices, suggesting future improvements to enhance reliability and performance.

2. Experimental

2.1. Film fabrication and analysis

For the TDTR analysis sample, amorphous GT films with a thickness of 30 nm and 100 nm were deposited on a Si substrate through co-sputtering of GeTe and Te targets to analyze the thermal properties of amorphous and crystalline GT films. The 30 nm amorphous GT film underwent heat treatment in a vacuum atmosphere at 473 K for 30 min using a rapid thermal annealing system (Real). Similarly, amorphous SGT films with a thickness of 50 nm and 100 nm were prepared on a Si substrate through co-sputtering of Se-doped GeTe and Te targets. Subsequently, TiN and Au layers with thicknesses of 50 nm and 100 nm, respectively, were deposited via sputtering.

To determine the crystallinity of the annealed GT thin film, XRD analysis (D/MAX-2500/PC, Rigaku) was conducted. For determining the thermal properties of GT and SGT thin films, TDTR analysis (N8-200 model, TMX Scientific™) was utilized. Short-duration pumping pulses were directed onto the thin film to induce heating in the targeted area, followed by the application of probing pulse for extended periods. Over time, the heat generated by the heating pulse decayed and led to changes in the reflectivity of the reflected probing pulse. By observing these reflectivity changes over time, properties such as the thermal conductivity of the thin film and interfacial thermal resistance between the thin films can be calculated.

2.2. Device fabrication and characterization

For electrical measurement and TTI analysis, a 50-nm-thick bottom electrode of Pt was deposited on a SiO_2/Si substrate using radio-frequency magnetron sputtering. For the GT-based OTS device, an amorphous GT film with a thickness of 100 nm was deposited by co-sputtering of GeTe and Te targets. Similarly, for the SGT-based OTS device, an amorphous SGT film of 50 nm was deposited by co-sputtering of the Se-doped GeTe and Te targets. Finally, a 30 nm TiN layer and a 50 nm Au layer were sputtered sequentially as the top electrodes.

DC voltage sweeps were measured using a Semiconductor parameter analyzer (HP 4155B). For electric pulse-based measurement, an arbitrary function generator (AFG 3102, Tektronix) and oscilloscope (TDS 3032B, Tektronix) were used. During measurements, the Pt bottom electrode (BE) was grounded.

To map thermal behavior during TS, TTI (NT220 Series, Microsanj™) analysis was performed. During pulse application to the DUT to induce heating, laser pulses were applied to the DUT, and the reflected light was captured by a CCD camera. By utilizing the change in thermal reflectance due to induced heating, thermal mapping during pulse application was achieved. The pixel size of the CCD camera was approximately 55 nm, and the spatial resolution was down to ~250 nm. The LED illumination time was adjusted during pulse application to enable thermal mapping at specific time intervals. Sequential analysis was performed using time-enabled *in-situ* analysis. A schematic of this setup is shown in Fig. S2.

The thermal hotspots identified through TTI analysis were further examined using focused ion beam (Helios™ 5 UX, Thermo Scientific™) milling. Cross-sectional analysis was performed using TEM (NEO ARM, JEOL). Subsequent analyses, including FFT, STEM, and EDS, were conducted using this equipment. TEM and EDS analysis were performed at the Korea Basic Science Institute using the JEOL Monochromated ARM-200F (NEO-ARM, DJ105) operated at 200 kV with a dual SDD EDS system.

2.3. Electrothermal simulations

To understand the internal temperature during TS operation and the device failure process during the *in-situ* analysis, we conducted Electrothermal (ET) simulations. We utilized COMSOL Multiphysics and employed a heat-conduction model. To facilitate comparison with actual surface temperature measurements, we designed a planar device structure: a 4×4 μm^2 area for GT-based OTS device and 10×10 μm^2 for SGT-based OTS device to mimic the actual device. The electrodes, substrate, and switching layer thickness were kept constant. The

simulations involved determining of the thermal conductivity, electrical conductivity, density, relative permittivity, and heat capacity of each layer. These properties were extracted from experimental results and references.

3. Results

3.1. GT-based OTS devices

TTI analysis is used to determine thermal mapping during the operation of GT-based OTS devices. Subsequently, the *in-situ* TTI analysis is verified by findings that imply time-sequenced thermal mapping during voltage application. Following TTI analyses, we confirmed the device's failure based on transmission electron microscopy (TEM) analysis of the heated area and applied time-domain thermoreflectance (TDTR) analysis to obtain the thermal properties necessary for ET simulations. ET simulations were conducted to analyze internal temperatures during TS operation and the device failure process during *in-situ* analysis.

A cross-point structure was fabricated with a stack of Au (50 nm)/TiN (30 nm)/GT (100 nm)/Pt (50 nm), where the junction area of the cross-point was 16 μm^2. A schematic of the device is illustrated in Fig. 1 (a). Au, known for its high thermal reflectance coefficient, was used to enhance the accuracy of the TTI analysis [46]. For the same reason, Au was deposited on top of the sample with a GT layer. Fig. 1(b) presents the current (*I*)–voltage (*V*) graph of the fabricated OTS device, demonstrating typical TS behavior: after applying the electroforming voltage (V_f) of 2.1V, threshold voltage (V_{th}) value of 2 V and hold voltage (V_{hold}) of 1.9 V were observed with a compliance current of 0.1 mA. Subsequently, a pulse of 2 V with a duration of 1 μs was applied to induce TS behavior, as depicted in Fig. 1(c). To suppress current overflow after TS behavior, an external resistor load equal to 2 kΩ was applied. During this

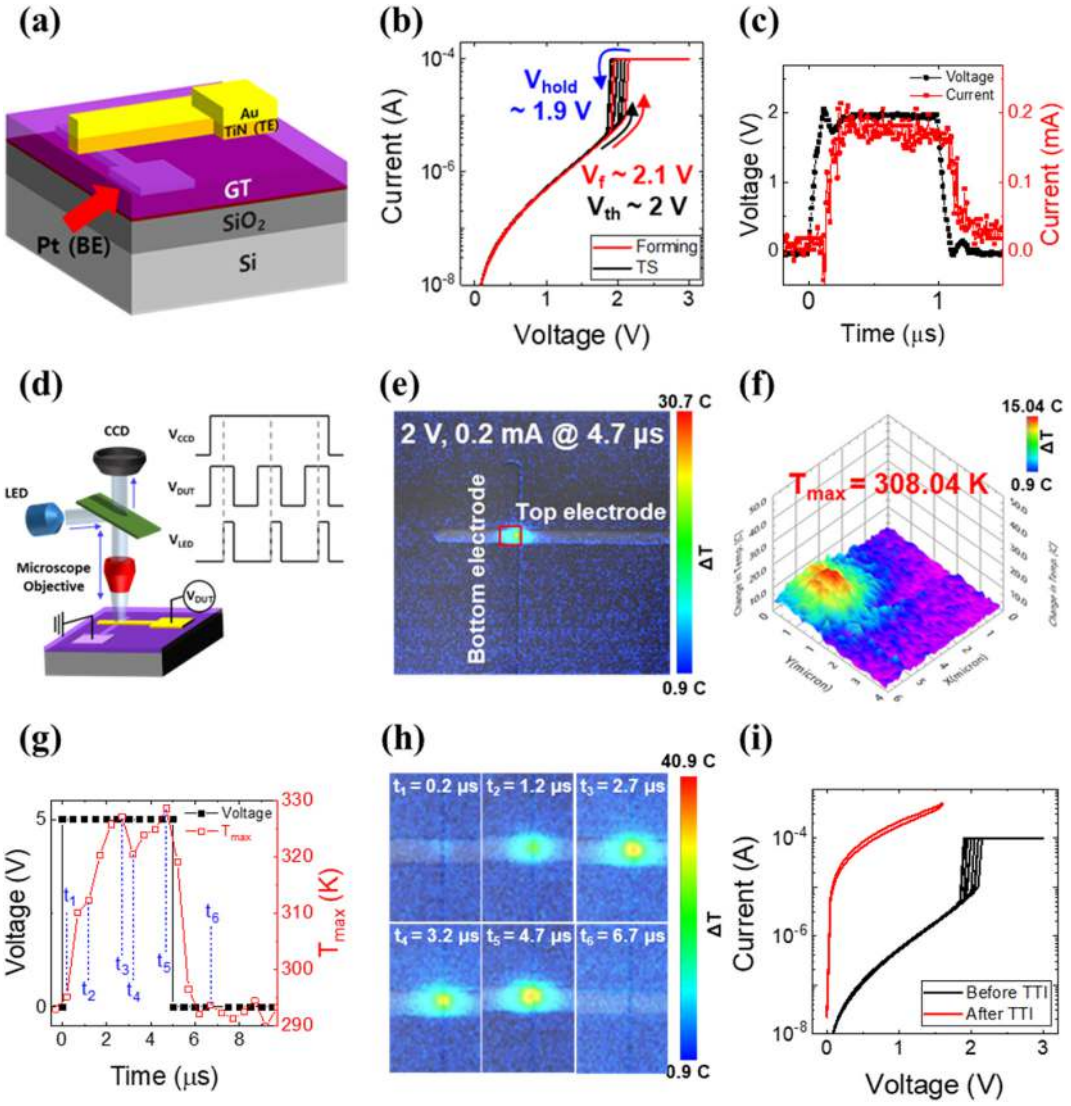

Fig. 1. (a) Schematic of a cross-point GeTe (GT) device, stacked with Au/TiN/GT/Pt. (b) Current (*I*)–voltage (*V*) curves of a GT device demonstrating threshold switching (TS) operation. After electroforming at ~2.1 V (V_f), TS occurred at ~2 V (V_{th}), and the device turned off at ~1.9 V (V_{hold}). (c) TS behavior was demonstrated using a pulse measuring system with an applied pulse (amplitude = 2 V, duration = 1 μs). To limit current, an external resistor load of 2 kΩ was applied. (d) Schematic of thermoreflectance thermal imaging (TTI) analysis showing a thermal image during the application of an external pulse. (e) Thermal image of GT device during pulse application. A current of approximately 0.2 mA was observed with a 2 V pulse, confirming TS occurrence as compared to the *I–V* curve. (f) Three-dimensional temperature mapping of the junction area in the device. The maximum temperature (T_{max}) of 308.04 K was observed with a localized heating spot, indicating TS occurred through a conductive channel (CC). (g) Time-voltage-temperature graph of *in-situ* TTI. The graph shows an increase in T_{max}, followed by a decrease and subsequent increase, likely due to device deformation during analysis. (h) Thermal images during *in-situ* analysis from t_1 (0.2 μs) to t_6 (6.7 μs) are noted in (g). (i) *I–V* curves before and after TTI analysis. Device failure during TTI analysis was expected.

pulse application, a current of approximately 0.2 mA was observed.

Transient TTI analysis aimed to obtain thermal images during the TS operation of the fabricated device. While a voltage pulse sufficient to induce TS was applied to the device under test (DUT), the LED illuminated the device, and the resulting thermal mapping on the device surface was captured using a charge-coupled device (CCD) camera, as depicted in the schematic in Fig. 1(d). Fig. 1(e) shows the transient thermal temperature (T_{max}) of the mapping image observed during the application of a pulse with a 2 V amplitude and an amplitude of 5 μs using TTI analysis. As shown in the figure, the top and bottom electrode lines respectively parallel to the x- and y-axes overlap, defining the working area of the junction.

During TTI analysis, a thermal mapping image was observed with a 2 V pulse amplitude and 5 μs duration. The measured device current was approximately 0.2 mA which is consistent with the I-V characteristics shown in Fig. 1(b) and (c), confirming the anticipated occurrence of TS. Notably, Fig. 1(e), illustrates a distinct hot spot with a diameter of less than 1 μm within the junction area, supported by the surface temperature distribution illustrated in Fig. 1(f), which varies based on the junction's position. This observation strongly suggests that the hot spot originates from TS behavior. To further confirm that the hot spot arises specifically due to TS, we conducted TTI analysis both before and after the electroforming process. As shown in Fig. S3, the emergence of the hot spot was only observed after forming, indicating that it is indeed triggered by TS behavior. Supporting this interpretation, previous studies using conductive-atomic force microscopy have reported an increase in high-current density in localized regions of OTS device after the electroforming process [47,48], along with the presence of localized conducting path or CCs [49]. Based on these reports, to our knowledge, the presence of CC has been directly observed in localized regions of the actual device structure during TS events. These findings suggest that the observed hot spots during TS events are activated CCs within the device.

To assess the lateral confinement of the CC, we analyzed surface temperature line profiles obtained from high-resolution TTI measurements. As shown in Fig. S4, the region of maximum surface temperature was consistently confined within a ~300 nm-wide region, indicating localized heating consistent with CC formation. This observation is not limited by the spatial resolution of the TTI system (~250 nm), thus supporting the presence of a laterally confined CC. A more quantitative determination of the CC geometry will be provided later using ET simulations.

Following confirmation of TS operation based on transient TTI analysis, *in-situ* TTI analysis investigated thermal mapping over time during pulse applications. The timing of LED illumination was adjusted during voltage pulse application on the DUT to sequentially connect transient TTI analysis results throughout the pulse duration for *in-situ* TTI analysis. Fig. S2 illustrates the schematic of the *in-situ* TTI analysis. To observe device failure due to heating, a 5 V voltage pulse was applied, and thermal mapping was conducted using LED pulses at 500 ns intervals during the pulse. Temporal voltage and temperature graphs during the *in-situ* analysis are illustrated in Fig. 1(g), with the maximum temperature (T_{max}) extracted from thermal images. Results of the *in-situ* analysis are presented in Fig. S5 and supplementary video. Temperature increased from t_1 to t_3, followed by a decrease at t_4 and subsequent increase until t_5. The temperature returned to 293.15 K, pre-pulse application, at t_6 after removing the external pulse. The thermal mapping results at times t_1–t_6 are displayed in Fig. 1(h). At t_1, localized heating in the low-temperature range was observed, suggesting an off-state, while the presence of CC was confirmed even in the off-state. Thermal images from t_2 to t_5 in Fig. 1(h) illustrate varying heating regions, possibly due to changes in CC or film properties during TS. To confirm the reproducibility of these thermal features, we also performed repeated in-situ TTI measurements on multiple GT devices, as shown in Fig. S6. A hot spot was consistently observed in the electrode region upon TS, as confirmed by repeated measurements. Additionally, a transient decrease in temperature was repeatedly observed during the middle of the applied pulse, which will be further discussed in a later section. Furthermore, transient TTI analysis at 5 V after the *in-situ* analysis indicated increased electrical conductivity of the device and surface T_{max}, as illustrated in Fig. S7. This suggests device deformation likely occurred during the *in-situ* analysis. A direct current sweep was conducted after the TTI analysis, depicted in Fig. 1(i), with resistance and electrical conductivity values listed in Table S1. Increased electrical conductivity and the absence of TS behavior suggest impending device failure.

The failure attributed to increased conductivity was caused by crystallization occurring within the device during *in-situ* analysis. To assess whether changes in the film occurred after the analysis, TEM analysis of the heating area was performed to observe the device cross-section (Fig. S8). The TEM cross-section of the heating area, illustrated in Fig. 2(a), reveals a crystalline phase extending over 900 nm accompanied by thin-film shrinkage. This cross-section can be divided into three distinct regions, as depicted in Fig. 2(b)–(d). Fig. 2(b) illustrates a region with deformation and shrinkage in film thickness, where the minimum thickness between the electrodes was measured at 25 nm. Fast Fourier Transform (FFT) analysis confirmed the presence of crystalline phases within the GT thin film. Similarly, Fig. 2(c) verifies the existence of crystalline phases and slight shrinkage within the GT thin film. In both regions, the Te crystal structure was identified. Detailed observations of these are provided in this study. In contrast, Fig. 2(d) highlights an area where the GT remained amorphous without film deformation. Comparing these findings to the cross-sectional TEM image of the as-deposited device, Fig. S8 demonstrates similarities to Fig. 2(d), characterized by the absence of crystallization. This suggests that device failure resulted from localized crystallization. Fig. 2(e)–(j) presents the energy-dispersive spectroscopy (EDS) analysis of Ge and Te in the regions shown in Fig. 2(b)–(d). Fig. 2(i) and (j) illustrates the uniform distribution of Ge and Te, while Fig. 2(e)–(h) reveals the phase separation of Ge and Te in the crystalline region. The elemental distribution in the crystalline regions is further detailed in Fig. S8.

In the region illustrated in Fig. 2(b), Te predominantly accumulated in the upper part of the device. This phenomenon was attributed to electromigration (EM) of Te, induced by the positive bias voltage applied from the top electrode, which caused Te, with its high electronegativity to migrate [50]. Additionally, EDS elemental mapping confirmed that the region where Te accumulated coincided with areas that experienced significant shrinkage. This observation suggests that EM occurs in regions where the electric field and Joule heating are concentrated, along with crystallization. Consequently, failure in the GT device was inferred to result from repeated pulse applications, leading to crystallization and phase separation. Further discussion on the correlation between crystallization and phase-separation phenomena is provided. In contrast, the EDS results in Fig. 2(c) indicate that Ge remained concentrated at the center of the film, while Te migrated outward (to both the upper and lower regions), exhibiting a segregated morphology that suggests material separation independent of the voltage direction. This implies a different crystallization trend compared to Fig. 2(b), indicating that crystallization occurred due to Joule heating during device operation. Crystallization in regions without concentrated electric fields occurred because of heat transfer from the generated CC to the surrounding areas. Thus, two pathways of failure were identified: (1) crystallized regions with high Te concentration migrated toward the upper part of the device, and (2) crystallized regions formed as Te migrated both upper and lower parts from the initial region. Although both crystallization modes were experimentally observed, it was not possible to determine which played a dominant role or occurred earlier during the failure process. Therefore, to gain further insight into the relative importance and sequence of these mechanisms, ET simulations were conducted by evaluating the thermal conditions under electrical stress.

TEM analysis confirmed the presence of amorphous GT (a-GT) and crystalline GT (c-GT) films. Additionally, to comprehensively

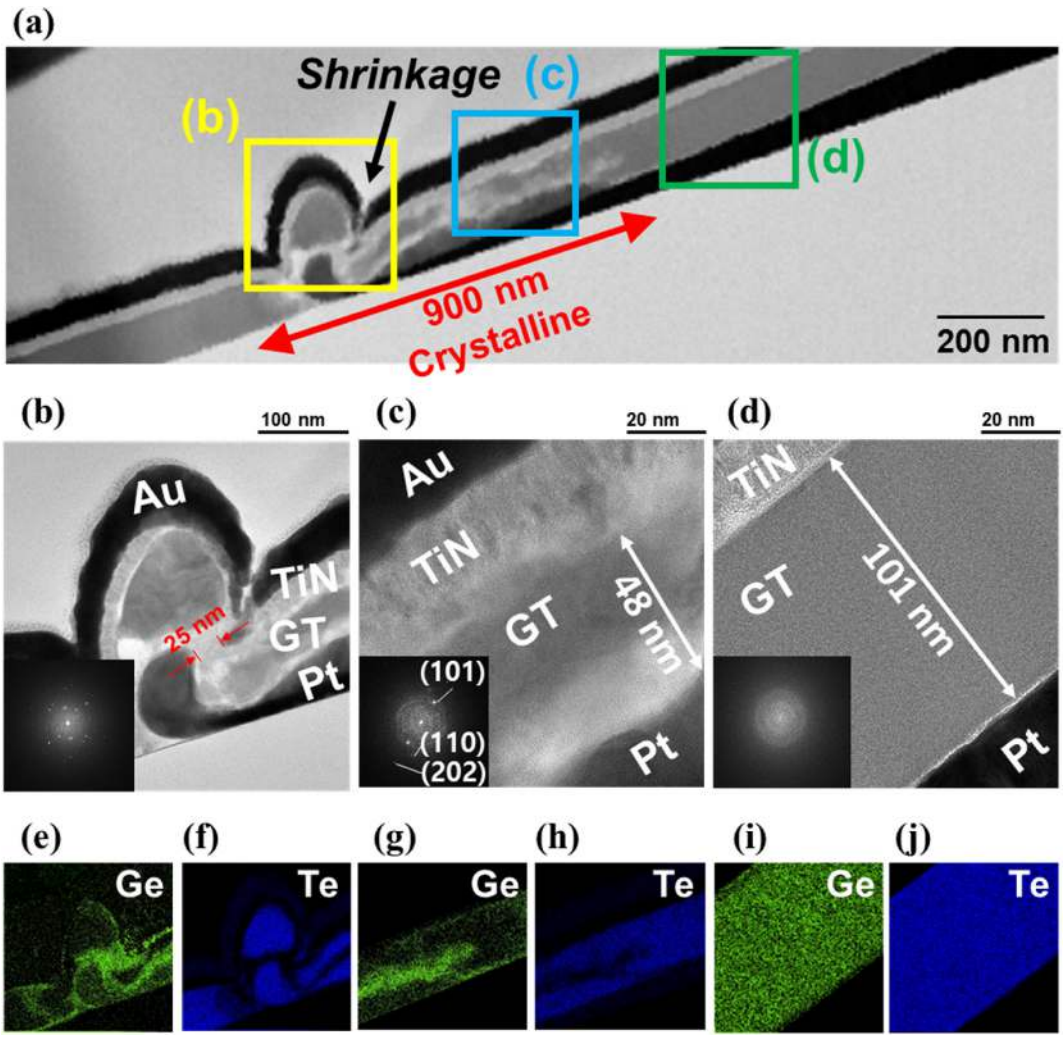

Fig. 2. (a) The transmission electron microscopy (TEM) image shows the heating region. Fast Fourier Transform (FFT) analysis confirmed the presence of a crystalline phase over a region of 900 nm. Three distinct regions are identified in this TEM image, labeled as (b), (c), and (d), respectively. (b) Crystalline region, where the crystalline GT layer was confirmed, along with device deformation and film shrinkage. (c) Crystalline region with slight device shrinkage; the crystalline GT layer was similarly confirmed. (d) Amorphous region without shrinkage. It is expected that localized crystallization caused device failure. (e)–(j) TEM–Energy dispersive spectroscopy (EDS) analysis results for Ge and Te elements corresponding to the regions (b)–(d). Element segregation was observed in crystallized films.

understand the internal temperature during the TS operation of the OTS device and the failure process during *in-situ* analysis, the thermal properties of both amorphous and crystalline were needed.

To obtain these properties, three types of GT thin films were prepared: 30-nm- and 100-nm-thick a-GT (based on the actual thickness of the device), and 20-nm-thick c-GT (obtained by annealing the 30-nm-thick a-GT). This thickness corresponded to the device's minimum crystallization thickness, found to be 25 nm in Fig. 2(b). The c-GT film was annealed at 200 °C for 30 min after deposition. XRD analysis was performed to verify the crystalline phase after annealing, as shown in Fig. 3(a). This figure demonstrates that the films were initially amorphous and crystallized after heat treatment. Using the Joint Committee on Powder Diffraction Standards (JCPDS), the presence of the Te crystal phase in the c-GT film was confirmed. These results are consistent with the FFT analysis results in the inset of Fig. 2(b).

TDTR analysis was used to determine the thermal properties of the prepared films. Au/TiN/GT/Si stack samples were prepared, and the film thicknesses, thermal properties of Si substrate, and thermal boundary resistance of Au/TiN are shown in Figs. S9 and S10, and Table S2. Fig. 3(b) illustrates a schematic of the TDTR analysis. The thermal decay curves of the samples are in Fig. 3(c), where the x-axis represents time and the y-axis represents the amplitude of the reflected light, which decreases time. The decay rate of the reflected light amplitude in the c-GT was faster than that in the 30-nm-thick a-GT, indicating the higher thermal conductivity of the c-GT. Additionally, the slowest decay rate of the 100-nm-thick a-GT film is attributed to its thickness. The thermal conductivity and interfacial thermal resistance between the TiN electrodes and the GT films were calculated by fitting the TDTR thermal decay curves of the samples, as shown in Fig. 3(d). The thermal conductivities of a-GT (30 nm and 100 nm) and c-GT (20 nm) were approximately 0.14, 0.15, and 0.45 W m^{-1} K^{-1}, respectively. This confirms the higher thermal conductivity of the c-GT and the trend of increasing thermal conductivity with increasing thickness of the a-GT. The thermal boundary resistances of TiN/GT were 28.5, 27.15, and 23.79 m^2 K GW^{-1}, respectively, similar to values reported in the literature for chalcogenide film thermal conductivity and thermal boundary resistance (Fig. S10 and S11) [41,51–53].

Based on the results of the TTI and TEM analyses, we confirmed the presence of CC due to localized hotspots and device failure (crystallization and phase separation) caused by heating. Additionally, from the electrical measurements and TDTR, we observed increases in electrical and thermal conductivities after crystallization. These findings guided our prediction of the device's internal temperatures during TS operation and our understanding of the failure process during *in-situ* analysis using

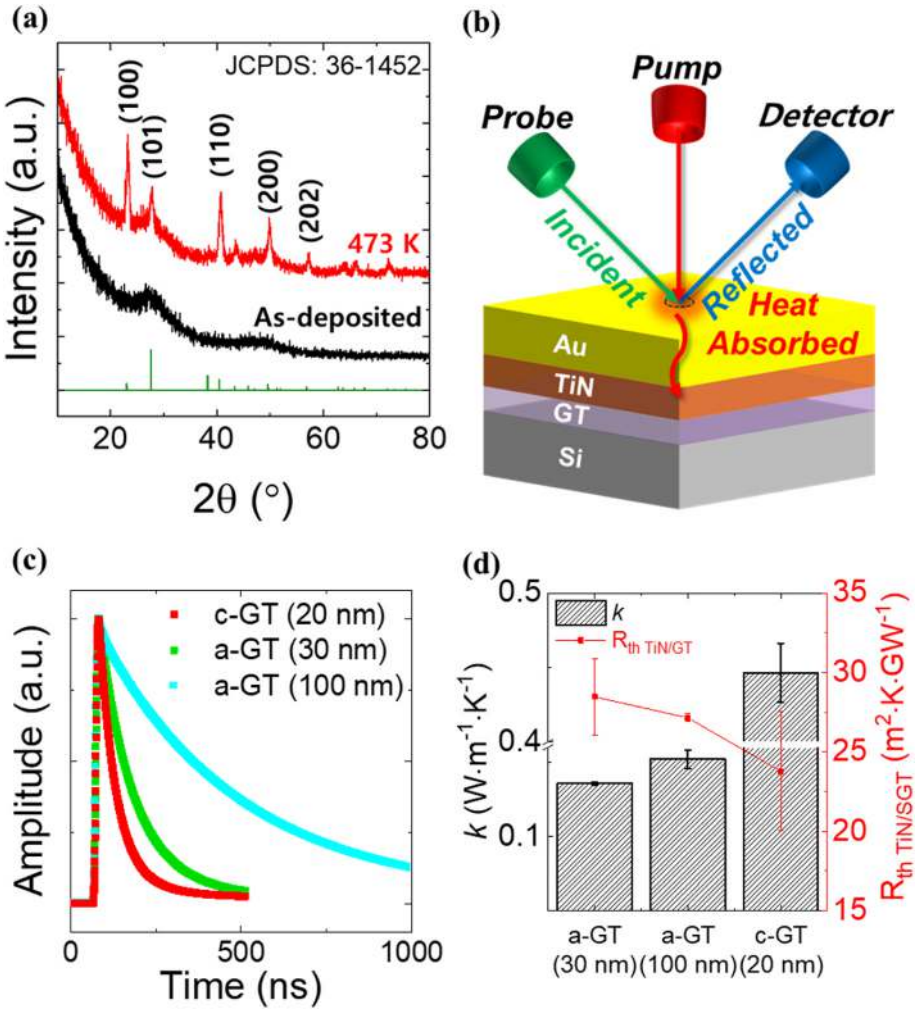

Fig. 3. (a) X-ray diffraction results of amorphous GT (a-GT) films as-fabricated and crystalline GT (c-GT) films annealed at 200 °C for 30 min. Te metal peaks were confirmed in the annealed GT thin film. (b) Schematic of time-domain thermoreflectance (TDTR) analysis. (c) TDTR results of the a-GT (30 nm and 100 nm) and c-GT (20 nm). The thermal decay rate of c-GT is faster than that of a-GT (30 nm), attributed to the higher thermal conductivity of c-GT. The slower decay rate observed in a-GT (100 nm) is due to its increased thickness. (d) Calculated thermal conductivities and thermal boundary resistances of a-GT and c-GT (20 nm). The thermal conductivities of a-GT (30 and 100 nm) and c-GT were approximately 0.14, 0.15, and 0.45 W m^{-1} K^{-1}, respectively. The thermal boundary resistance values were 28.5, 27.15, and 23.79 m^2 K GW^{-1}.

ET simulations. The parameters required for the simulation are listed in Table S3. A simulation strategy is first necessary to predict the internal temperature. Fig. 4(a) illustrates the simulation strategy. We adjusted variables such as the size of the CC and crystallization onset to ensure that the surface T_{max} calculated from the simulations closely matched the observed surface T_{max} from the TTI analysis. We then aimed to determine the internal T_{max} values calculated from the simulations.

To predict the internal temperature of a device during TS operation, it is essential to consider the shape, properties, and size of the CC. Previous studies have investigated various CC shapes [47,49]; however, a cylindrical CC was introduced to simplify the modeling process. Additionally, the mechanism underlying the TS phenomenon within the OTS device was considered to define the CC. Several theories on the operating mechanisms, such as the thermal runaway [54,55] and field-induced nucleation [56–58], have been proposed to explain the TS phenomenon in OTS. However, these models are based on insufficient evidence: negative differential resistance was not implemented, electronic properties were not adequately integrated, and material conductivity was insufficiently considered.

In contrast, electrical models have emerged as a promising mechanism to address these challenges and have gained considerable attention [38,47,48,59]. In these models, the forming process induces localized trap-rich regions within the amorphous matrix, primarily through the generation and accumulation of valence alternation pairs (VAPs) [60]. These VAPs act as metastable defect states formed via bond rearrangement under strong electric fields, modulating the local electronic structure without altering the material phase. The resulting inhomogeneous defect landscape facilitates field-driven carrier transport during TS, without involving any structural transformation.

To investigate the intrinsic behavior of TS, we focused on SGT devices, which offer improved thermal stability. Our TTI and subsequent TEM analyses of these structures revealed that the hot spot region remained amorphous, even after repeated switching events—supporting the electronic origin of the switching process.

This observation reinforces the core assumption of the electrical model: that the conductive path is transient, electronic in nature, and not accompanied by any structural phase change during TS. Accordingly, we characterized CC as an electronic filament formed via field-induced conductivity modulation within the amorphous matrix, which serves as the basis for the ET simulation modeling presented in the subsequent section.

Due to the challenges in observing the size of CC caused by its volatility, we chose to employ this strategy. Simulations were conducted for various CC sizes to identify the size at which the surface T_{max} aligned

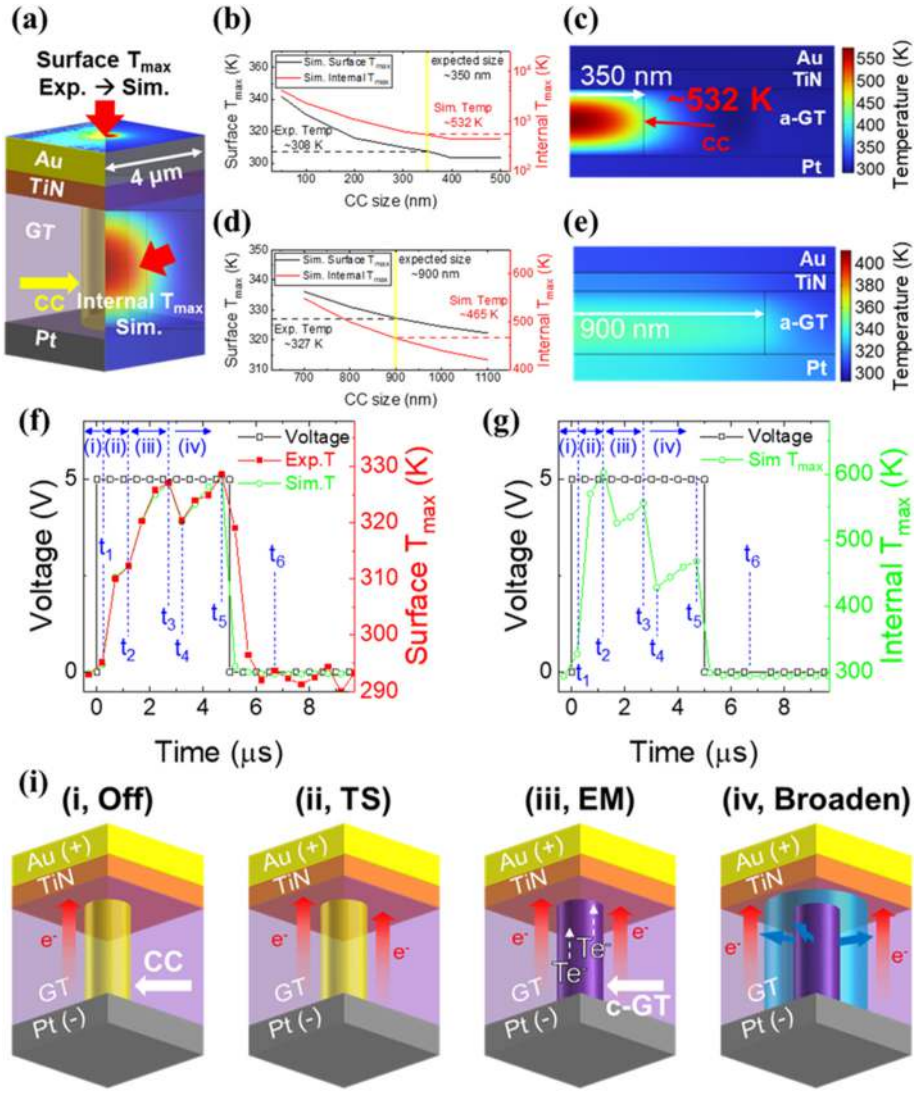

Fig. 4. (a) The electrothermal (ET) simulation strategy involves adjusting unknown parameters to match the maximum surface temperature observed in TTI analysis results, to understand the internal temperature and failure process. (b) Size screening of the CC under the same TS conditions as those in Fig. 1(e). The CC diameter is approximately 350 nm, and the maximum internal temperature (internal T_{max}) reaches 532 K. (c) Cross-sectional image of ET simulation for Fig. 4(b). (d) Size screening of the CC under the conditions of Fig. 1(g) at t_5 (4.7 μs). The CC diameter is approximately 900 nm, and the maximum internal temperature reaches 465 K. (e) Cross-sectional image of ET simulation for Fig. 4(d). (f) Voltage and temperature graphs on the device surface obtained from *in-situ* TTI analysis as a function of time, comparing experimental and simulation results. (g) Simulated internal T_{max} of GT during *in-situ* analysis. (h) Schematic of the failure process during *in-situ* analysis. Up to t_1, the device remains in the off state. At t_2, TS occurs; after t_2, crystallization occurs without further changes in the CC size. This process involves crystallization occurring alongside electromigration. At t_4, failure is expected due to an increase in CC size caused by crystallization in the surrounding area as a result of Joule heating.

with the TTI analysis results (**Figure S 12**). Subsequently, the internal temperature at that point was determined. The simulation results for these conditions are shown in Fig. 4(b). As the CC size increased, both the surface T_{max} and internal T_{max} decreased. However, the rate of decrease differed significantly. While the surface T_{max} showed a gradual decline, the internal T_{max} decreased exponentially. This pronounced decrease is attributed to the low thermal conductivity setting assigned to the CC, which leads to strong thermal confinement and limited heat dissipation within the conductive region. The simulated surface T_{max} of 308 K, matching the TTI result, was obtained when the CC diameter was 350 nm—closely corresponding to the ~300 nm lateral size observed in Fig. S4. At this point, the internal T_{max} was estimated to be 532 K. As shown in Fig. 1(f), the surface temperature increase appears to be limited to approximately 15 K, whereas simulation results suggest that the internal temperature of the amorphous layer can reach up to 532 K under typical switching conditions. This apparent discrepancy is likely attributed to the low thermal conductivity of the amorphous GT layer, which is thought to confine most of the heat within the film and suppress its escape to the surface. A similar trend has been reported in RRAM devices, where SThM measurements revealed only modest surface heating (~20 K), despite simulations indicating internal filament temperatures exceeding 1000 K. This observation supports the notion that low surface temperature signals can still be consistent with filamentary conduction [39]. Fig. 4(c) shows a cross-sectional image obtained during the simulation under these conditions. The central region of the CC exhibited the highest heat generation, with temperatures exceeding 400 K across the entire area. This temperature is sufficient to induce degradation of the component, similar to or higher than the previous annealing temperature of 473 K. However, due to the absence of crystallization, it was inferred that the pulses applied were too short to induce crystallization. It was also noted that repeated operation of the component under these conditions could lead to degradation. In

summary, based on our modeling, we predicted that when TS occurs (with a current of 0.2 mA at 2 V) with a diameter of 350 nm forms, the internal temperature could increase to 532 K. We then simulated the internal temperature during the *in-situ* analysis to understand the failure process.

To simulate the failure process during *in-situ* analysis, the following additional assumptions were necessary for modeling the internal temperature during TS operation: 1) changes in the size of the CC and 2) changes in electrical conductivity during thermal analysis and crystallization. We first describe the strategies used to adjust these variables.

The variation in the CC size was considered. Previous simulations indicated the presence of a 350 nm CC during TS occurrence; however, TEM analysis revealed a crystallized area of 900 nm. Upon adjusting the CC properties to match those of the c-GT, we conducted simulations with a size of 900 nm, which yielded a surface T_{max} similar to that of the actual analysis results, as shown in Fig. 4(d). This suggests that the crystalline region, once crystallized, function as the CC due to its high electrical conductivity. Fig. 4(e) shows a cross-sectional image from the simulation under crystallized CC. Consequently, the CC size boundary was inferred to range from 350 nm to 900 nm. Fig. 4(b) and (d) confirm that increasing the CC size reduces heat generation. Thus, during *in-situ* analysis, we aimed to increase the CC size when the surface T_{max} decreased; to minimize variables, we expanded the CC size accordingly.

Second, the changes in electrical conductivity and the timing of crystallization during thermal analysis were considered. Regarding electrical conductivity, Fig. S7 shows a difference in device resistance before and after the *in-situ* analysis. Based on these results, the device resistance boundary during the *in-situ* analysis was determined, and the variables were adjusted to increase the electrical conductivity of the CC. Furthermore, due to continuous heating during the *in-situ* analysis, it was expected that once crystallization occurred, it would persist. In other words, we aimed to identify the point at which the properties of CC transitioned to those of c-GT. An increase in the thermal conductivity of the CC led to a simultaneous rise in surface temperature and a decrease in the internal temperature. Thus, it was inferred that crystallization occurred when the internal temperature increased anomalously (Fig. S13). By adjusting these variables, a surface T_{max} similar to that in the *in-situ* analysis results was calculated, as shown in Fig. 4(f). The time points t_1–t_6 from Fig. 1(g) are directly marked in Fig. 4(f).

Through the alignment of the experimental and simulation results in Fig. 4(f), the temporal states of the *in-situ* analysis results can be understood as follows: up to t_1: (i) off-state; t_1–t_2: (ii) occurrence of TS; t_2–t_3: (iii) EM with crystallization, and t_3 onward: (iv) broadening of CC. Additionally, the internal T_{max} value during this process was confirmed, as shown in Fig. 4(g). As mentioned previously, the low heat generation at t_1 indicates an off-state. Subsequently, the temperature from t_1 to t_2, matches the transient TTI analysis results, indicating the occurrence of TS. Furthermore, it was confirmed that the internal heating temperature increased from 570 K to 602 K during the TS. This indicates an increase in the device current due to heating during TS, which is expected to accelerate device degradation. After t_2, CC crystallization was confirmed. Moreover, two distinct states, namely (iii) and (iv), were observed based on the CC diameters of 350 nm and 900 nm. Based on previous findings (Figs. S8 and 2(d)), it was confirmed that 1) crystallization occurred concurrently with the EM phenomena, and 2) peripheral crystallization occurred due to CC heating. In case (iii), crystallization was expected to occur in the 350 nm area where the electric field was concentrated. Conversely, in (iv), crystallization was expected to occur across the 900 nm region due to heat transfer to the periphery. Thus, increased internal heating during TS led to CC crystallization concurrent with the EM phenomena. Subsequently, heating from repeated pulse applications led to an increased crystallization area around the CC periphery. These processes are illustrated schematically in Fig. 4(i). A mismatch between the experimental and simulation results was observed, particularly after the pulse application. This discrepancy is likely due to a technical artifact in the in-situ TTI measurement setup. Specifically, the LED light source used for thermal imaging has a finite pulse width (~500 ns), which can overlap with the trailing edge of the electrical pulse. This timing mismatch results in apparent post-pulse heating artifacts, even though the applied voltage has already ceased.

3.2. SGT-based OTS devices

As aforementioned, the study was conducted on the SGT-based OTS device, which exhibits excellent thermal stability, using the same approach applied to the GT-based OTS device. This section focuses on a comparative interpretation of the electrical, thermal, and structural characteristics of SGT-based devices, leveraging the methodologies established in Section 3.1. The SGT-based OTS device was fabricated with a cross-point structure identical to that of the GT-based OTS device, comprising Au (50 nm)/TiN (30 nm)/SGT (50 nm)/Pt (50 nm), with a junction area of 100 μm^2. The thickness and area of the SGT device were carefully selected based on experimental results obtained under various device conditions, in order to exhibit device characteristics comparable to those of the GT device. Further details regarding the characteristics of the SGT devices are presented in Fig. S14–S16.

Fig. 5(a) presents the I-V curve of the fabricated SGT-based OTS device, showing typical TS behavior: after the application of 2.7 V of V_f, a V_{th} of 1.65 V and a V_{hold} of 1.55 V were observed with a compliance current of 10 μA. Although the V_f for the SGT device was higher than that for the GT device, the operating voltage was lower, which can be attributed to the thinner SGT film. Subsequently, a 3 V pulse with a 5 μs duration was applied to induce TS behavior, as shown in Fig. 5(b). To limit the current, an external resistor of 2 kΩ was used, similar to the GT-based OTS device. During this application, a current of approximately 0.25 mA was observed. The endurance test results (Fig. 5(c)) demonstrated that the SGT-based OTS devices reliably operated for up to 10^{12} cycles, highlighting their excellent endurance characteristics. This superiority can be attributed to the SGT film's enhanced thermal stability. Accordingly, TTI analysis was conducted on the SGT-based OTS device in the same manner as for the GT-based OTS device to investigate its thermal behavior. As expected, superior thermal properties were observed. Fig. 5(d) shows the transient thermal mapping image obtained during the application of a pulse with a 5 V amplitude and a duration of 90 μs. A current of 0.25 mA was measured, and, like the GT-based OTS device, a distinct hot spot with a diameter of less than 1 μm was observed within the junction area. This observation was corroborated by the surface temperature distribution illustrated in Fig. 5(e), which varies based on the junction's position. The T_{max} at this time was 299.28 K, lower than the 308.04 K observed for the GT-based OTS device with a shorter pulse. To verify the consistency of thermal behavior across different devices, we conducted additional TTI measurements on various SGT devices, which exhibited consistent temperature profiles. An in-situ TTI experiment was also performed on another SGT device with a different structural configuration. Both results are presented in Fig. S17.

While the temperatures observed in the TTI analysis correspond to the device's surface temperature, as shown in Fig. 4, predicting the internal heating temperature through ET simulations is necessary. However, even a comparison of surface temperatures demonstrates that the Joule heating effects in SGT-based OTS devices are significantly lower. Given that the GT devices suffered from thermally induced degradation likely caused by high Joule heating and EM, this reduction in SGT may help suppress similar breakdown events. The I–V characteristics of the same SGT device before and after TTI analysis, including the forming step, are shown in Fig. 5(f). These DC measurements clearly demonstrate that TS behavior is preserved after thermal imaging, although the V_{th} decreases slightly from 1.9 V to 1.4 V, accompanied by an increase in off-state current. This degradation is attributed to minor device wear induced by repeated operation. The corresponding TTI results for this device, including thermal images acquired before and during the voltage pulse, are provided in Fig. S18.

Importantly, while a localized hot spot is observed during the pulse

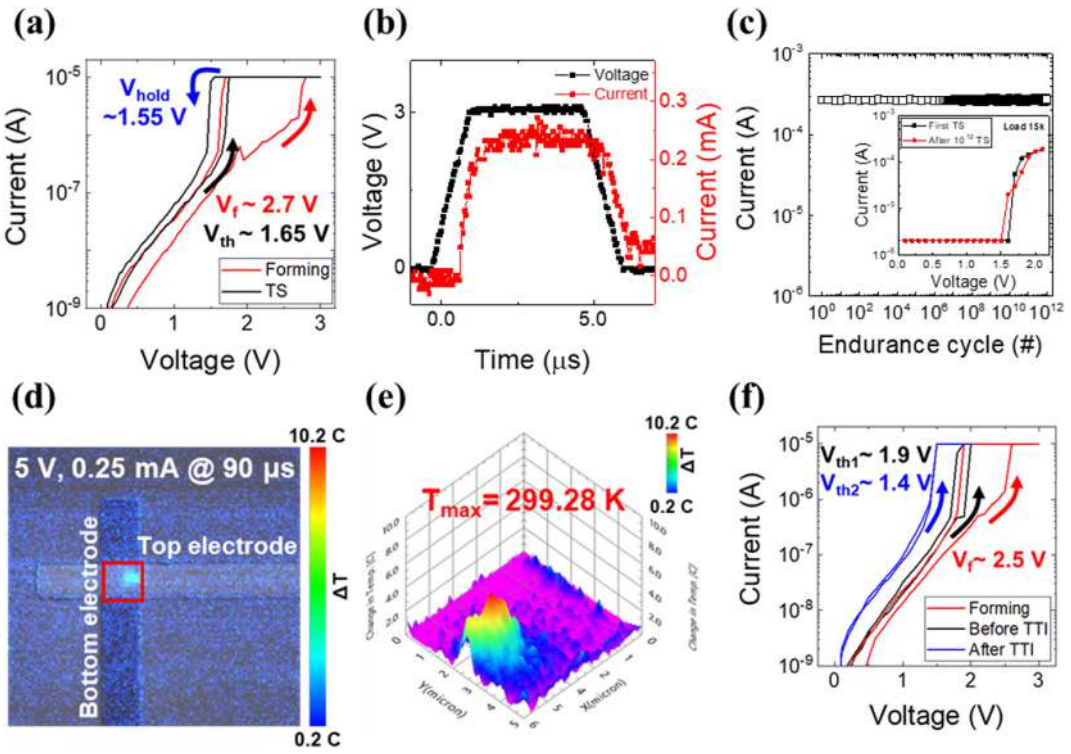

Fig. 5. (a) The I-V curves of the SGT device demonstrate the threshold switching (TS) operation. After the electroforming process at ~2.7 V (V_f), TS occurred at ~1.65 V (V_{th}), and the device turned off at ~1.55 V (V_{hold}). (b) TS behavior was demonstrated using a pulse measurement system when a pulse (amplitude = 3 V, duration = 5 μs) was applied. To limit the current, an external resistor load of 2 kΩ was used. (c) Endurance cycle test of the SGT device showing stable on-current over 10^{12} pulses (main), and preserved TS behavior before and after cycling (inset), confirming excellent endurance and switching reliability. (Pulse condition: 3 V unipolar pulses with a pulse width of 100 ns and a pulse period of 200 ns) (d) A thermal image of SGT device during pulse application. When a 5V pulse was applied, a current of ~0.25 mA was observed, confirming TS occurrence when compared with the pulse measurement results. (e) Three-dimensional temperature mapping of the junction area in the device revealed a maximum temperature (T_{max}) of 299.28 K with a localized heating spot, consistent with the GT thermal mapping result (Fig. 1(f)). (f) DC I–V characteristics of the same SGT device before and after TTI analysis, including the forming step. The TS behavior is clearly preserved, confirming that the device remained operational following thermal analysis. The corresponding TTI results for this device, including thermal images before and during pulse application, are provided in Fig. S18.

application (Fig. S18(c)), the device retains its TS functionality afterward. This reinforces the conclusion that hotspot formation does not necessarily indicate device failure but is instead a manifestation of localized Joule heating associated with TS operation. Furthermore, the current magnitude observed during the TTI analysis is comparable to that measured in the DC I–V curve (Fig. 5(a)) and pulse-based measurement (Fig. 5(b)), suggesting that the thermal signal captured during TTI corresponds to the TS occurrence. Motivated by the thermal behavior observed in the TTI analysis, we next performed TEM analysis to investigate whether the hotspot region exhibited any structural modifications.

TEM analysis was conducted to investigate the structural characteristics of the heat-generating region. During the FIB processing, however, the top electrode detached, resulting in the absence of Au and TiN materials in the heat-generating region. Fig. 6(a) displays the TEM analysis results, which confirm that the SGT thin film is amorphous throughout the region, as evidenced by FFT analysis. Additionally, TEM-EDS analysis results for Ge, Se, and Te elements are illustrated in Fig. 6 (b)–(d). These results indicate that the three elements are uniformly distributed, contrasting with observation in GT-based OTS devices where EM phenomena were detected. This difference suggests the presence of Ge-Se bonds (2.14 eV per bond, ~207 kJ/mol) with higher bond energy than Ge-Te bonds (1.53 eV per bond, ~148 kJ/mol) in the SGT thin film, enhancing resistance to EM phenomena [61,62]. Consequently, the high bonding energy of the SGT thin film may contribute to improved thermal stability, reducing the likelihood of device failure.

Simultaneously, the Joule heating effect during TS operation in the SGT-based OTS device was analyzed. The internal temperature expectations were determined through ET simulations, employing the same methodology used for the GT-based OTS device.

Prior to this, the thermal properties of the SGT thin film were obtained through TDTR analysis, conducted similarly to the analysis for the GT thin film. For the SGT thin film, only amorphous thin films were analyzed, as no crystalline phase was observed during operation of the SGT-based OTS device. Additionally, to enhance accuracy, TDTR analysis was performed using SGT thin films of 50 nm and 100 nm thickness (Fig. S10, Table S2). The results, shown in Fig. 6(e), indicate a faster thermal decay rate for the 50 nm thin film. Based on these results, extracted thermal properties are presented in Fig. 6(f). The thermal boundary resistance values were 28.9 and 28.93 m^2 K·G·W^{-1} for the 50 nm and 100 nm thin films, respectively, confirming that interfacial characteristics were independent of the thickness of the SGT thin film. In contrast, thermal conductivity values were 0.14 and 0.153 W m^{-1} K^{-1}, respectively, showing a slight increase with greater thickness. These results and trends are similar to those for GT thin films (0.14 and 0.15 W m^{-1} K^{-1} for 30 nm and 100 nm amorphous GT thin films), indicating minimal differences in the thermal properties of the two thin films. This confirms that the high thermal stability of the SGT thin film, due to its high bonding energy, influences its higher crystallization temperature compared to the GT device [37], while having minimal impact on thermal conductivity or thermal boundary resistance. In terms of thermal conductivity within OTS devices, SGT thin films are expected to exhibit lower thermal conductivity due to their thinner thickness, thereby slowing heat dissipation.

Therefore, to analyze the effect of the low thermal conductivity of the SGT thin film on the internal temperature during TS operation, ET

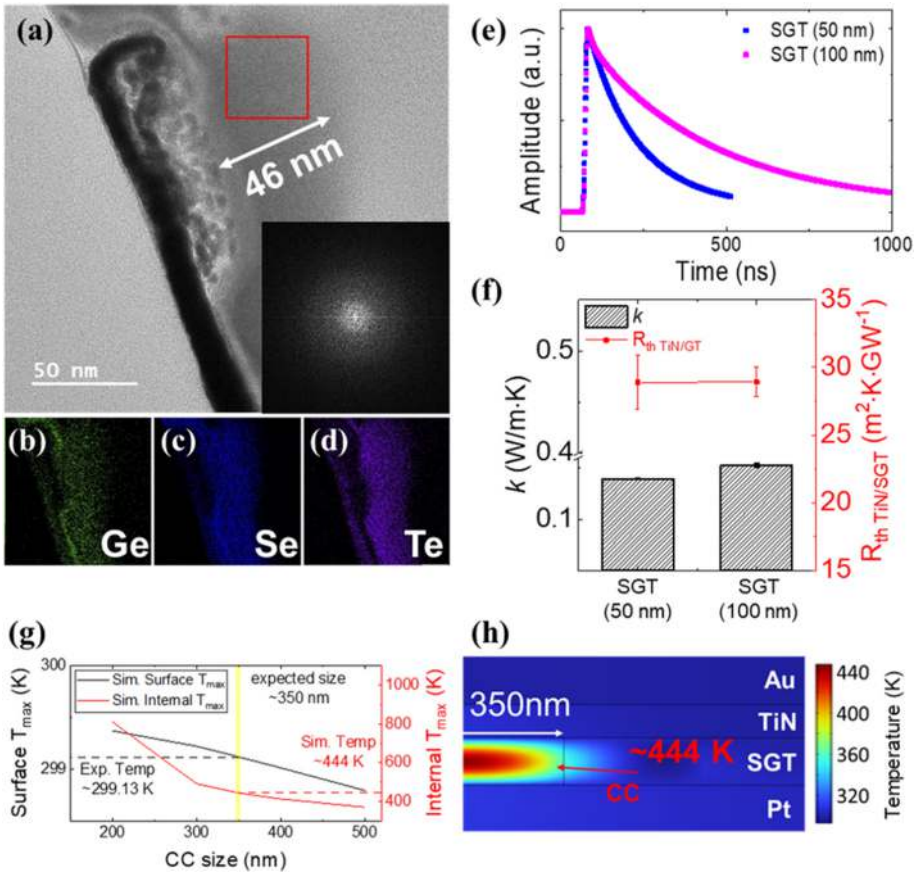

Fig. 6. (a) TEM image demonstrating the heating region of SGT device. Unlike the GT results, FFT analysis confirmed the presence of an amorphous phase throughout the entire region. (b)–(d) TEM-EDS analysis results for Ge, Se, and Te elements corresponding to region (a), showing that each element was evenly distributed. (e) TDTR results for SGT thin films with thicknesses of 50 nm and 100 nm. The faster decay rate observed in the SGT 50 nm is attributed to its reduced thickness. (f) Calculated thermal conductivities and thermal boundary resistances of SGT thin films with thicknesses of 50 nm and 100 nm. The thermal conductivities of 50 nm and 100 nm SGT were approximately 0.14 and 0.153 W m^{-1} K^{-1}, respectively. The thermal boundary resistance values were 28.9 and 28.93 m^2 K GW^{-1}, respectively. (g) Size screening of the CC under the same TS conditions as those shown in Fig. 5(d). The CC diameter was approximately 350 nm, similar to that of the GT device, with an internal T_{max} reaching 444 K. (h) Cross-sectional image of the ET simulation corresponding to Fig. 6(g). Compared to the GT device (~532 K), the SGT device exhibited a lower internal T_{max}.

simulations were conducted following the same methodology. By adjusting the CC size and comparing the TTI analysis results of the TS operation process with the ET simulation results, the CC size in the SGT device was estimated. Fig. 6(g) presents the ET simulation result after varying the CC size. Notably, the surface temperature aligned with the TTI analysis results when the CC diameter was approximately 350 nm, consistent with the ET simulation results of the GT-based OTS device. This finding indicates that during OTS device operation, TS operation can be expected within a CC diameter of 350 nm under TTI analysis conditions. Furthermore, the internal T_{max} under these CC conditions was determined to be approximately 444 K, which is lower than the ET simulation results for the GT-based OTS device. This is attributed not to the high thermal conductivity of the SGT thin film, but rather to its lower electrical conductivity, resulting in reduced Joule heating.

In summary, the SGT-based OTS device demonstrated enhanced resistance to EM phenomena, attributed to the high bonding energy of the SGT thin film and reduced Joule heating due to its lower electrical conductivity. To improve the durability of OTS devices, two strategies can be employed: (1) suppressing EM by increasing the thin film's bonding through elemental doping, and (2) optimizing electrical properties to minimize Joule heating during TS operation by reducing the on-current. While electrical properties have a more significant effect on durability, the ET simulation results for the SGT-based OTS device indicated that the internal T_{max} increased by approximately 150 K— a level high enough to induce thermal stress during repeated operation. Moreover, the subtle structural/chemical changes caused by this Joule heating cannot be overlooked as contributing factors. Given the ongoing discussions about Joule heating effects in SOM devices, further research is necessary to quantitatively analyze its impact and clarify its interaction with electrical properties.

4. Conclusions

We fabricated and compared GT-based and SGT-based OTS devices using a cross-point architecture. Transient TTI analysis of both devices enabled direct observation of the conducting channel evolution during volatile TS and allowed determination of the associated heating temperatures. Specifically, for the GT-based OTS device, *in-situ* TTI analysis provided real-time videos of the heating process and surface temperature profiles over time, which were crucial for understanding the breakdown process. Subsequent TEM analysis identified the structural changes in the device after TS, confirming either the retention of the amorphous state or localized crystallization within the heating region. EDS and XRD analyses of the GT-based OTS device revealed that the EM of Te, induced by repetitive pulses and crystallization due to Joule heating, led to device failure. In contrast, the higher bonding energy in the SGT film appeared to suppress EM, contributing to enhanced device stability. To investigate the internal temperature during TS and the failure mechanisms, ET simulations were conducted using thermal properties derived from TDTR analysis. The TDTR results showed no

significant differences in thermal properties between GT and SGT films, indicating negligible disparities in heat dissipation effects. ET simulations revealed that during TS, a CC with a diameter of 350 nm formed in both GT- and SGT-based OTS devices, elevating the internal T_{max} to approximately 530 K and 444 K, respectively. Through the ET simulations of the *in-situ* TTI analysis of the GT-based OTS device, device failure was primarily attributed to high internal heating during TS, which caused EM and crystallization of Te induced by repetitive pulse operations, followed by peripheral crystallization due to heat transfer. The SGT-based OTS device demonstrated greater durability and stable operation compared to the GT-based OTS device, primarily due to higher bonding energy within the thin film and reduced Joule heating. Conversely, failures in the GT-based OTS device were caused by Te EM and crystallization triggered by repetitive pulse operations. These findings underscore the importance of strategies to suppress EM and minimize Joule heating to improve the durability of OTS devices.

Future research should focus on quantitatively analyzing the impact of Joule heating on the thermal and electrical properties of devices, as well as identifying subtle degradation factors that may also affect SGT-based devices. Further efforts should aim to improve the synchronization between optical and electrical signals in order to minimize timing artifacts in the TTI system and thereby enhance measurement accuracy. This study provides valuable foundational data to improve the performance and reliability of OTS devices.

CRediT authorship contribution statement

Ju Hwan Park: Writing – original draft, Visualization, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Hyun Wook Kim:** Writing – review & editing, Investigation. **Hyun Kyu Seo:** Writing – review & editing, Methodology, Investigation, Data curation. **Dustin Kendig:** Writing – review & editing, Visualization, Investigation. **Mohammad Shakouri:** Writing – review & editing, Visualization, Investigation. **Gun Hwan Kim:** Writing – review & editing, Investigation. **Jae Hyuck Jang:** Writing – review & editing, Investigation. **Min Kyu Yang:** Writing – review & editing, Supervision, Conceptualization. **Byung Joon Choi:** Writing – original draft, Supervision, Formal analysis, Conceptualization.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Byung Joon Choi reports financial support was provided by Korea Ministry of Trade Industry and Energy. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mtadv.2025.100602.

Data availability

Data will be made available on request.

References

[1] K.H. Kim, S. Gaba, D. Wheeler, J.M. Cruz-Albrecht, T. Hussain, N. Srinivasa, W. Lu, A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications, Nano Lett. 12 (2012) 389.
[2] D.B. Strukov, H. Kohlstedt, Resistive switching phenomena in thin films: materials, devices, and applications, MRS Bull. 37 (2012) 108.
[3] B. Sun, S. Ranjan, G. Zhou, T. Guo, Y. Xia, L. Wei, Y.N. Zhou, Y.A. Wu, Multistate resistive switching behaviors for neuromorphic computing in memristor, Mater. Today Adv. 9 (2021) 100125.
[4] Y. Kim, W.H. Jeong, S.B. Tran, H.C. Woo, J. Kim, C.S. Hwang, K.S. Min, B.J. Choi, Memristor crossbar array for binarized neural networks, AIP Adv. 9 (2019) 045131.
[5] G.W. Burr, R.S. Shenoy, K. Virwani, P. Narayanan, A. Padilla, B. Kurdi, H. Hwang, Access devices for 3D crosspoint memory, J. Vac. Sci. Technol. B Nanotechnol. Microelectron. Mater. Process. Meas. Phenom. 32 (2014) 040802.
[6] Q. Xia, J.J. Yang, Memristive crossbar arrays for brain-inspired computing, Nat. Mater. 18 (2019) 309.
[7] Y.C. Bae, A.R. Lee, G.H. Baek, J.B. Chung, T.Y. Kim, J.G. Park, J.P. Hong, All oxide semiconductor-based bidirectional vertical p-n-p selectors for 3D stackable crossbar-array electronics, Sci. Rep. 5 (2015) 13362.
[8] S. Kim, D.I. Moon, W. Lu, D. Hwan Kim, D. Myong Kim, Y.K. Choi, S.J. Choi, Latch-up based bidirectional npn selector for bipolar resistance-change memory, Appl. Phys. Lett. 103 (2013) 033505.
[9] W.Y. Park, G.H. Kim, J.Y. Seok, K.M. Kim, S.J. Song, M.H. Lee, C.S. Hwang, A Pt/TiO_2/Ti Schottky-type selection diode for alleviating the sneak current in resistance switching memory arrays, Nanotechnology 21 (2010) 195201.
[10] G.H. Kim, J.H. Lee, J.H. Han, S.J. Song, J.Y. Seok, J.H. Yoon, K.J. Yoon, M.H. Lee, T.J. Park, C.S. Hwang, Schottky diode with excellent performance for large integration density of crossbar resistive memory, Appl. Phys. Lett. 100 (21) (2012) 213508.
[11] L. Fu, K. Yang, X. Gao, X. Song, Z. Wu, X. Fan, Y. Li, Anatomy of high-uniform unidirectional volatile switching behavior in SiO_2/TiO_2-based selection device, Mater. Today Adv. 13 (2022) 100197.
[12] B.J. Choi, J. Zhang, K. Norris, G. Gibson, K.M. Kim, W. Jackson, M.X.M. Zhang, Z. Li, J.J. Yang, R.S. Williams, Trilayer tunnel selectors for memristor memory cells, Adv. Mater. 28 (2016) 356.
[13] B. Govoreanu, C. Adelmann, A. Redolfi, L. Zhang, S. Clima, M. Jurczak, High-performance metal-insulator-metal tunnel diode selectors, IEEE Electron Device Lett. 35 (2014) 63.
[14] K. Virwani, G.W. Burr, R.S. Shenoy, C.T. Rettner, A. Padilla, T. Topuria, P.M. Rice, G. Ho, R.S. King, K. Nguyen, A.N. Bowers, M. Jurich, M. BrightSky, E.A. Joseph, A. J. Kellock, N. Arellano, B.N. Kurdi, K. Gopalakrishnan, Sub-30nm scaling and high-speed operation of fully-confined access-devices for 3D crosspoint memory based on mixed-ionic-electronic-conduction (MIEC) materials, 2012 Int. Elect. Dev. Meet. 2 (2012) 7.1–72.7.4.
[15] D. Chu, S. Kang, G. Kim, J. Sung, J. Lim, Y. Choi, D. Han, C. Shin, First integration of Ni barrier layer for enhanced threshold switching characteristics in Ag/HfO_2-based TS device, Mater. Today Adv. 22 (2024) 100492.
[16] M. Jo, Y.W. Seo, H. Yoon, Y.S. Nam, S.Y. Choi, B.J. Choi, J. Son, Embedded metallic nanoparticles facilitate metastability of switchable metallic domains in Mott threshold switches, Nat. Commun. 13 (2022) 4609.
[17] W.C. Chien, C.W. Yeh, R.L. Bruce, H.Y. Cheng, I.T. Kuo, C.H. Yang, A. Ray, H. Miyazoe, W. Kim, F. Carta, E.K. Lai, M.J. Brightsky, H.L. Lung, A Study on OTS-PCM pillar cell for 3-D stackable memory, IEEE Trans. Electron. Dev. 65 (2018) 5172.
[18] S.R. Ovshinsky, Reversible Electrical Switching Phenomena in Disordered Structures, Cambridge University Press, 1968.
[19] S. Ban, H. Choi, W. Lee, S. Hong, H. Zang, B. Lee, M. Kim, S. Lee, H. Lee, T. Kim, Pulse dependent threshold voltage variation of the ovonic threshold switch in cross-point memory, IEEE Electron Device Lett. 41 (2020) 373.
[20] T. Ravsher, D. Garbin, A. Fantini, R. Degraeve, S. Clima, G.L. Donadio, S. Kundu, H. Hody, W. Devulder, J. Van Houdt, V. Afanas'ev, R. Delhougne, G.S. Kar, Polarity-induced threshold voltage shift in ovonic threshold switching chalcogenides and the impact of material composition, Phys. Status Solidi RRL 17 (2023) 2200417.
[21] I.M. Park, K.W. Lee, J.H. Park, S.J. Song, T.Y. Kim, Z. Wu, W.J. Lee, B.D. Choi, Y. J. Jeong, S.C. Oh, K. Park, B.J. Kuh, Y.J. Song, Y.G. Shin, J.H. Song, Enhanced endurance characteristics in high performance 16nm Selector Only Memory (SOM), in: 2023 Technical Digest – International Electron Devices Meeting (IEDM), 2023, pp. 1–4.
[22] J. Yi, M. Kim, J. Seo, N. Park, S. Lee, J. Kim, G. Do, H. Jang, H. Koo, S. Cho, S. Chae, T. Kim, M.-H. Na, S. Cha, The chalcogenide-based memory technology continues: beyond 20nm 4-deck 256Gb cross-point memory, in: 2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), 2023, pp. 1–2.
[23] T. Kim, H. Choi, M. Kim, J. Yi, D. Kim, S. Cho, H. Lee, C. Hwang, E.R. Hwang, J. Song, S. Chae, Y. Chun, J.K. Kim, High-performance, cost-effective 2z nm two-deck cross-point memory integrated by self-align scheme for 128 Gb SCM, in: 2018 IEEE International Electron Devices Meeting (IEDM), 2018, pp. 37.1.1–37.1.4.
[24] S. Jia, H. Li, T. Gotoh, C. Longeaud, B. Zhang, J. Lyu, S. Lv, M. Zhu, Z. Song, Q. Liu, J. Robertson, M. Liu, Ultrahigh drive current and large selectivity in GeS selector, Nat. Commun. 11 (2020) 4636.
[25] Z. Zhao, S. Clima, D. Garbin, R. Degraeve, G. Pourtois, Z. Song, M. Zhu, Chalcogenide ovonic threshold switching selector, Nano-Micro Lett. 16 (2024) 81.

[26] S. Jia, H. Li, Q. Liu, Z. Song, M. Zhu, Scalability of sulfur-based ovonic threshold selectors for 3D stackable memory applications, Phys. Status Solidi RRL 15 (2021) 2100084.
[27] M. Lee, S. Lee, M. Kim, S. Lee, C. Won, T. Kim, C. Kwon, K. Yoon, J. Lee, H. Kim, T. Lee, $Ge_{1-x}S_x$ chalcogenide alloys for OTS applications using magnetron sputtering, J. Alloys Compd. 930 (2023) 167409.
[28] B. Govoreanu, G.L. Donadio, K. Opsomer, W. Devulder, V.V. Afanas'ev, T. Witters, S. Clima, N.S. Avasarala, A. Redolfi, S. Kundu, O. Richard, D. Tsvetanova, G. Pourtois, C. Detavernier, L. Goux, G.S. Kar, Thermally stable integrated Se-based OTS selectors with >20 MA/cm2 current drive, >3.103 half-bias nonlinearity, tunable threshold voltage and excellent endurance, in: 2017 Symposium on VLSI Technology, 2017, pp. T92–T93.
[29] Y. Koo, K. Baek, H. Hwang, Te-based amorphous binary OTS device with excellent selector characteristics for x-point memory applications, in: 2016 IEEE Symposium on VLSI Technology, 2016, pp. 1–2.
[30] M. Anbarasu, M. Wimmer, G. Bruns, M. Salinga, M. Wuttig, Nanosecond threshold switching of $GeTe_6$ cells and their potential as selector devices, Appl. Phys. Lett. 100 (2012) 143505.
[31] D. Seong, S.Y. Lee, H.K. Seo, J.W. Kim, M. Park, M.K. Yang, Highly reliable ovonic threshold switch with TiN/GeTe/TiN structure, Materials 16 (2023) 2066.
[32] R. Wu, R. Gu, T. Gotoh, Z. Zhao, Y. Sun, S. Jia, X. Miao, S.R. Elliott, M. Zhu, M. Xu, Z. Song, The role of arsenic in the operation of sulfur-based electrical threshold switches, Nat. Commun. 14 (2023) 6095.
[33] H.Y. Cheng, W.C. Chien, I.T. Kuo, C.W. Yeh, L. Gignac, W. Kim, E.K. Lai, Y.F. Lin, R. L. Bruce, C. Lavoie, C.W. Cheng, A. Ray, F.M. Lee, F. Carta, C.H. Yang, M.H. Lee, H. Y. Ho, M. BrightSky, H.L. Lung, Ultra-high endurance and low I_{OFF} selector based on AsSeGe chalcogenides for wide memory window 3D stackable crosspoint memory, in: 2018 IEEE International Electron Devices Meeting (IEDM), 2018, pp. 37.3.1–37.3.4.
[34] X. Li, Z. Yuan, S. Lv, S. Song, Z. Song, Extended endurance performance and reduced threshold voltage by doping Si in GeSe-based ovonic threshold switching selectors, Thin Solid Films 734 (2021) 138837.
[35] T. Kim, D. Lee, J. Kim, H. Sohn, Firing voltage reduction in thermally annealed Ge–As–Te thin film with ovonic threshold switching, J. Vac. Sci. Technol. B Nanotechnol. Microelectron. Mater. Process. Meas. Phenom. 38 (2020) 032213.
[36] M.J. Lee, D. Lee, S.H. Cho, J.H. Hur, S.M. Lee, D.H. Seo, D.S. Kim, M.S. Yang, S. Lee, E. Hwang, M.R. Uddin, H. Kim, U.I. Chung, Y. Park, I.K. Yoo, A plasma-treated chalcogenide switch device for stackable scalable 3D nanoscale memory, Nat. Commun. 4 (2013) 2629.
[37] H.K. Seo, J.J. Ryu, S.Y. Lee, M. Park, S.G. Park, W. Song, G.H. Kim, M.K. Yang, Highly linear and symmetric ovonic threshold switches based on GeSeTe for high-density memory applications, Adv. Elect. Mater. 8 (2022) 2200161.
[38] D. Ielmini, Y. Zhang, Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices, J. Appl. Phys. 102 (2007) 054517.
[39] S. Deshmukh, M.M. Rojo, E. Yalon, S. Vaziri, C. Koroglu, R. Islam, R.A. Iglesias, K. Saraswat, E. Pop, Direct measurement of nanoscale filamentary hot spots in resistive memory devices, Sci. Adv. 8 (2022) eabk1514.
[40] I.M. Datye, M.M. Rojo, E. Yalon, S. Deshmukh, M.J. Mleczko, E. Pop, Localized heating and switching in $MoTe_2$-Based resistive memory devices, Nano Lett. 20 (2020) 1461–1467.
[41] E. Yalon, S. Deshmukh, M.M. Rojo, F. Lian, C.M. Neumann, F. Xiong, E. Pop, Spatially resolved thermometry of resistive memory devices, Sci. Rep. 7 (2017) 15360.
[42] K. Yazawa, D. Kendig, A. Shakouri, Time-resolved thermoreflectance imaging for thermal testing and analysis, in: 39th International Symposium for Testing and Failure Analysis, vol. 194, 2013.
[43] D. Kendig, A. Tay, A. Shakouri, Thermal analysis of advanced microelectronic devices using thermoreflectance thermography, in: 22nd International Workshop on Thermal Investigations of Ics and Systems (THERMINIC), 2016, pp. 115–120.
[44] S.K. Nandi, S.K. Das, Y. Cui, A. El Helou, S.K. Nath, T. Ratcliff, P. Raad, R. G. Elliman, Understanding modes of negative differential resistance in amorphous and polycrystalline vanadium oxides, ACS Appl. Mater. Interfaces 14 (2022) 21270.
[45] S. Kumar, Z. Wang, N. Davila, N. Kumari, K.J. Norris, X. Huang, J.P. Strachan, D. Vine, A.L.D. Kilcoyne, Y. Nishi, R.S. Williams, Physical origins of current and temperature controlled negative differential resistances in NbO2, Nat. Commun. 8 (2017) 658.
[46] T. Favaloro, J.H. Bahk, A. Shakouri, Characterization of the temperature dependence of the thermoreflectance coefficient for conductive thin films, Rev. Sci. Instrum. 86 (2015) 024903.
[47] S. Lee, J. Lee, M. Kwak, O. Mosendz, H. Hwang, Understanding of forming and switching mechanism using trap distribution model for ovonic threshold switch device, Appl. Phys. Lett. 118 (2021) 212103.
[48] Z. Chai, W. Zhang, R. Degraeve, S. Clima, F. Hatem, J.F. Zhang, P. Freitas, J. Marsland, A. Fantini, D. Garbin, L. Goux, G.S. Kar, Evidence of filamentary switching and relaxation mechanisms in Ge_xSe_{1-x} OTS selectors, in: 2019 Symposium on VLSI Technology, 2019, pp. T238–T239.
[49] J. Kim, W. Kim, J. Kim, H. Sohn, Locally formed conductive filaments in an amorphous Ga2Te3 ovonic threshold switching device, AIP Adv. 13 (2023) 035221.
[50] C. Kim, D. Kang, T.Y. Lee, K.H.P. Kim, Y.S. Kang, J. Lee, S.W. Nam, K.B. Kim, Y. Khang, Direct evidence of phase separation in $Ge_2Sb_2Te_5$ in phase change memory devices, Appl. Phys. Lett. 94 (2009) 193504.
[51] J.P. Reifenberg, K.W. Chang, M.A. Panzer, S. Kim, J.A. Rowlette, M. Asheghi, H.S. P. Wong, K.E. Goodson, Thermal boundary resistance measurements for phase-change memory devices, IEEE Electron Device Lett. 31 (2010) 56.
[52] J.P. Reifenberg, M.A. Panzer, S. Kim, A.M. Gibby, Y. Zhang, S. Wong, H.S.P. Wong, E. Pop, K.E. Goodson, Thickness and stoichiometry dependence of the thermal conductivity of GeSbTe films, Appl. Phys. Lett. 31 (2010) 56–58.
[53] F. Xiong, A.D. Liao, D. Estrada, E. Pop, Low-power switching of phase-change materials with carbon nanotube electrodes, Science. 332 (2011) 568.
[54] D.M. Kroll, Theory of electrical instabilities of mixed electronic and thermal origin, Phys. Rev. B 9 (1974) 1669.
[55] D.M. Kroll, Theory of electrical instabilities of mixed electronic and thermal origin. II. Switching as a nucleation process, Phys. Rev. B 11 (1975) 3814.
[56] V.G. Karpov, Y.A. Kryukov, I.V. Karpov, M. Mitra, Field-induced nucleation in phase change memory, Phys. Rev. B 78 (2008) 052201.
[57] V.G. Karpov, Y.A. Kryukov, S.D. Savransky, I.V. Karpov, Nucleation switching in phase change memory, Appl. Phys. Lett. 90 (2007) 123504.
[58] I.V. Karpov, M. Mitra, D. Kau, G. Spadini, Y.A. Kryukov, V.G. Karpov, Fundamental drift of parameters in chalcogenide phase change memory, J. Appl. Phys. 102 (2007) 124503.
[59] P. Fantini, N. Polino, A. Ghetti, D. Ielmini, Threshold switching by bipolar avalanche multiplication in ovonic chalcogenide glasses, Adv. Elect. Mater. 9 (2023) 2300037.
[60] A.V. Kolobov, P. Fons, Insights into the physics and chemistry of chalcogenides obtained from x-ray absorption spectroscopy, Semicond. Sci. Technol. 32 (2017) 123003.
[61] P. Armand, R. Escalier, M. Ramonda, M. Bigot, R. Arinero, A. Piarristeguy, Modulation of structural, optical, and dielectric properties of $GeTe_{1-x}Se_x$ amorphous films with the Se content x ($0 \leq x \leq 1$), Mater. Today Commun. 46 (2025) 112699.
[62] R. Shekhawat, H. Pamuluri, V. Erkkara Madhavan, K. Ramesh, Structural transformation and phase change properties of Se substituted GeTe, Sci. Rep. 11 (2021) 7604.