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Tech Note: TN-004

THERMAL CHRACTERIZATION OF HIGH-POWER IN-LINE TRANSISTOR ARRAYS

Thermal performance is an especially important design consideration in the design of high power devices and components. Excessive heating on any portion of the power device can have an adverse effect on device performance and long-term reliability. The analysis and understanding of the thermal characteristics is increasingly more challenging with shrinking dimensions and more complex topologies prevalent in present day power devices. This Tech Note illustrates the capabilities of transient thermoreflectance thermal imaging in meeting these challenges.

The example selected to demonstrate this capability is a power MOSFET array designed for high voltage and high current operation at speeds in the megahertz range. Each FET in the array has a gate width of 100 microns. Sets of 15 parallel FETs are connected in rows or "cells." Cells are connected in parallel to create the final array with a desired size and effective channel width. The shortest array (1270 microns) has 12 parallel cells. The longest array (3175 microns) has 30 cells. The source and drain of each FET in the array is accessed by a planar network of fingers and vias made from aluminum metallization and oxide insulation layers. The top Al layer source finger is common to the source contact of each FET in the underlying array. Similarly, the top drain finger connects all the drains. The top fingers are each 115 microns wide. The gates of each FET are connected to a single poly-silicon layer. Gate, drain, source, and substrate probing is accomplished by means of contacts at the top and bottom of the array. The device structure is illustrated in Figure 1.

Figure 2a shows the thermal image for a 3.18 mm power array at a drain voltage = 0.5 V and a drain current = 0.5 A for a current density of 6 A/mm^2. The power density for this relatively low bias is about 10 W/cm^2.

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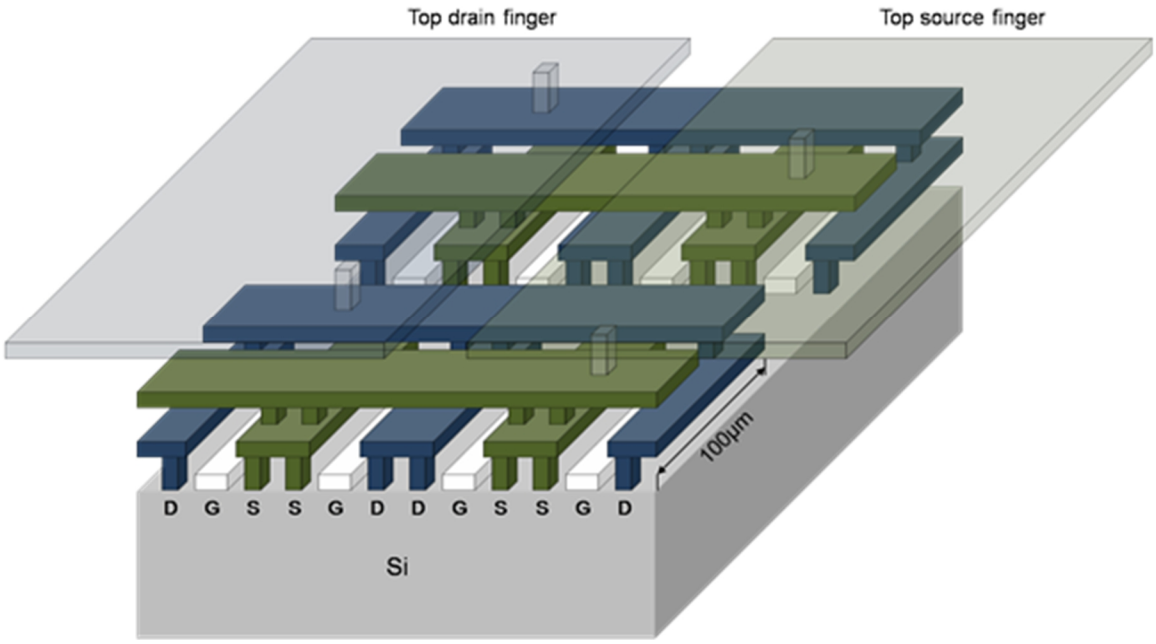

Figure 1: Structure for high-power MOSFET array

The current flowing through the source/drain contact network and through the individual transistors results in Joule heating which spreads laterally into the adjoining substrate. Figure 2b shows the temperature profile parallel to the long axis, a-a', of the array at this bias level. The profile was taken thru-the substrate on the surface of the silicon adjoining the source finger. This flat, smooth surface provides a good indication of the temperature distribution along the length of the array. The passivation layer and non-planar surfaces make the optical measurement of the temperature distribution on the metallic top surface 'noisy' and hence, more difficult to analyze.

The maximum temperature change is about 0.6 °C at the end of the array near the source contact. Thermocouple point measurements on the metal finger in the same region measured 1.3 °C. At this low bias level we observe a temperature trend in the array that is hotter toward the ends of the array and cooler near the middle.

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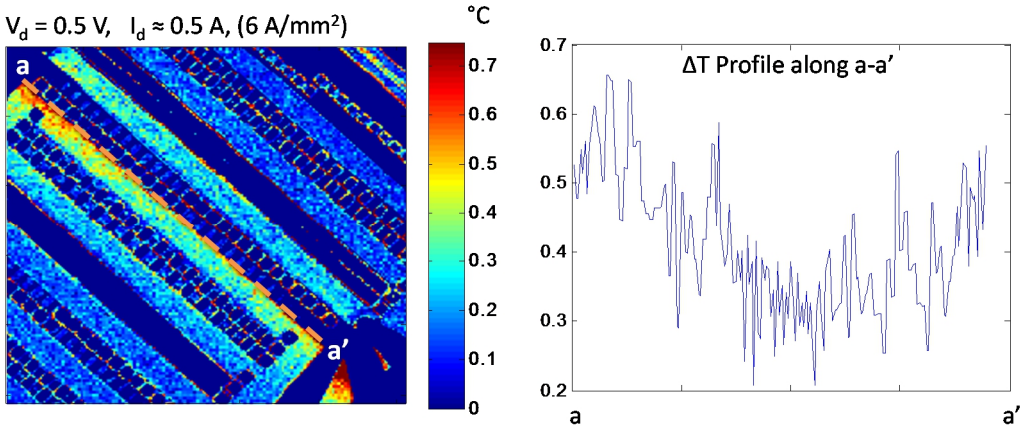

Figure 2: a) Thermal image for 3.2 mm array and b) Temperature profile along a-a'

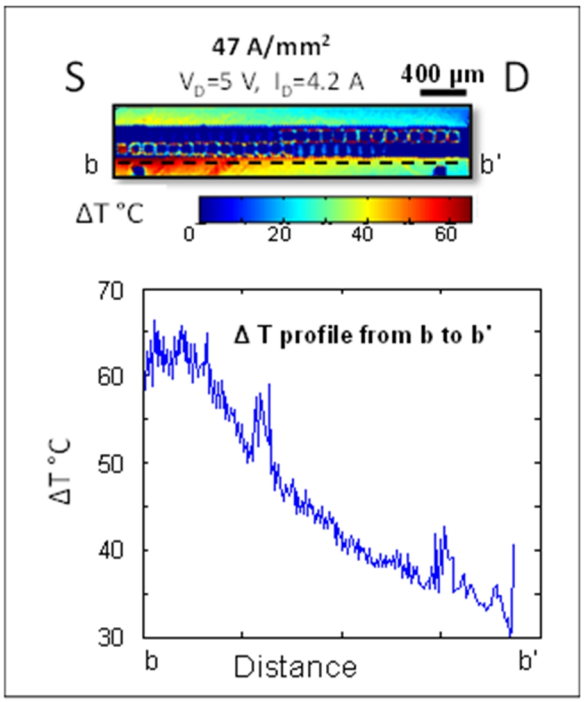

Figure 3: Thermal image of array at higher bias and temperature profile along b-b'

At higher bias levels, the thermal pattern of the array changes. At V_d=5 V and I_d=4.2 A the power density is 2645 W/cm^2 and the channel current density is 47 A/mm^2. Thermal imaging at this bias level shows the hottest part of the array rises 63 °C. Figure 3 shows that at the higher bias level heating becomes concentrated at one end of the array. The shift in dominant heating from both ends of the array for low bias to one end at high bias implies a change in the current distribution due to temperature-dependent electrical and thermal conductivities in the metallization layer as well as the temperature-dependence of the transistor characteristics.

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Although the detailed mechanism for the change in the current flow patterns may not be known, it is important to know that the changes do occur. This behavior indicates to the designer that temperature-dependent device and material properties play a key role in determining the current distribution and that a set of self-consistent electro-thermal calculations may be needed to completely analyze the thermal behavior of the device under high bias conditions.

Summary

This tech note briefly describes an application for analyzing temperature rise and temperature distributions in power transistor arrays under varied bias conditions using a Microsanj Nanotherm Series Thermoreflectance Thermal imaging System. The ability to characterize and understand the thermal behavior of power devices is extremely important for the prediction of safe operating limits and for determining the appropriate trade-offs between performance and long-term reliability.

References:

If there is interest in acquiring further details on the example described in this note, the reader is referred to reference [1].

[1] Thermal Characterization of High Power Transistor Arrays, K. Maize et al, *25th IEEE SEMI-THERM Symposium*, 2009.

